Wideband Inductorless Low-Noise Amplifier Using Three Feedback Paths

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Abstract- This paper presents the design of a wideband inductorless low noise amplifier (LNA) in 0.18 μm CMOS technology for multiband wireless communication standards. The LNA is a fully differential common-gate structure. It uses three feedback paths, for choosing arbitrary value of LNA transconductance which leads to a LNA with higher gain and lower noise figure (NF) over the previously reported amplifiers. Post-layout simulation results show a gain of 20.4 dB with a 3-dB bandwidth of 2.84GHZ, with a 2.62dB NF while dissipating 2.97mW. The IIP3 is -1.67dBm.

Index Terms- Inductorless, Low Noise Amplifier (LNA), Multistandard, Wideband.

I. INTRODUCTION

Nowadays, GSM, DECT, and GPS which are diverse wireless standards have been developed. It would be straightforward to integrate different wireless receivers together on a chip in order to satisfy the particular demands for each and every application; however, the required power consumption and chip area will be large. As a result, it is desirable to have a multi-standard receiver to meet all the mentioned standards. A wideband receiver is one of the possible solutions for multiband multi-standards receiver.

The Low Noise Amplifier (LNA) is nominated the first gain stage of a wideband receiver. It must meet several specifications simultaneously, which makes the design challenging. LNA should achieve good impedance matching, high, and flat gain, low noise figure (NF) across a wide frequency band, good linearity, and low area and power consumption.

With the help of several methods, wideband input matching for wideband amplifier can be achieved; such as using the distributed amplifier [1], [2], the filter-type amplifier [3], and the resistive shunt feedback amplifier [4], [5]. However these methods may suffer from various disadvantages such as high power consumption, large chip area, and inadequate NF.

One of the wideband LNA topologies that have been widely investigated is the common-gate low-noise amplifier (CGLNA) [7], [8]. A common-gate structure has better wideband input impedance matching than a common-source structure. Beside the simple input matching architecture (1/gm=Rs), the CGLNA also offers good linearity, stability, low power consumption, and robustness to PVT variation. However, its main drawback is the relatively high noise figure (NF) [6]. This is due to the tradeoff between the noise factor (F) and input impedance matching requirement (Zin=Rs).

In this paper, a gm-boosting scheme has been applied to a CGLNA to break the traditional link between the input matching and noise figure, and leads to a simultaneous reduction in noise and power dissipation in order to retain the advantages of the CG configuration and overcome its deficiencies. The use of three feedbacks improves the gain compared to all of the other CGLNA topologies. The whole structure is designed without the use of any bulky inductors, thus requires a less area. The presented LNA covers frequency bands for digital video broadcasting (DVB) at 450-850MHZ, global system for mobile communication (GSM) at 900MHZ, global positioning system (GPS) at 1.21 and 1.5 GHZ and cellular radios at 850-1900MHZ which provides a practical solution for multi-standard application. This paper is organized as follows. Section II reviews the gm-boosting technique by using negative feedback and section III discusses a new positive feedback with nmos transistor are discussed. The proposed circuit is presented in section IV then Section V presents post-layout simulation results and finally, section VI presents the conclusion and outline of this paper.

II. CIRCUIT DESCRIPTION

From Figure 1, which shows the differential CGLNA, gain and input impedance can be obtained as below:

\[ A_v = g_m R_L \] (1)

\[ R_{in} = \frac{2}{g_m} \] (2)

where \( g_m \) is the transconductance of M1. By assuming matching condition as \( R_{in} = 2R_s = 100\Omega \), the noise factor is given by

Figure 1: Differential CGLNA
In Equation 3, \( \gamma \) is the channel thermal noise coefficient \((1 < \gamma < 2)\), and \( a = g_m / g_{d0} \), is zero-bias drain conductance. By following the above equation, input matching condition force \( g_m \) to be equal to 20mS. In this condition, we cannot increase arbitrarily \( g_m \) for noise reduction. Therefore, gain can be increased through a gm-boosting technique which is suggested in Figure 2(a). Wherein inverting amplification, \( A \), is introduced between the source and gate terminal of M1, so that \( g_m \) is boosted to \( g_m (1 + A) \) and input impedance matching is given by:

\[
\frac{1}{g_m (1 + A_{NEG})} = R_s = 50\Omega
\]  

(4)

This configuration leads to smaller bias current, less channel noise from the input transistor M1, and consequently smaller noise contribution and power consumption. F which is given by

\[
F = 1 + \frac{\gamma}{1 + A_{NEG}} + \frac{aR_s}{R_L}
\]  

(5)

A capacitor-cross-coupling (CCC) is one of the possible ways to achieve passive inverting gain in this technique [6], [7], as shown in Figure 2(b), A is approximately given by the capacitor voltage division ratio

\[
A = \frac{c_2}{c_2 + c_{gs1}} = 1 + \frac{c_{gs1}}{c_{gs1}}
\]  

(6)

In Equation 6, \( c_{gs1} \) is the gate-source capacitance of M1. For \( C_1 >> C_{gs1} \), \( A \approx 1 \) and F simplifies from Equation 5 to 7:

\[
F = 1 + \frac{\gamma}{2a} + \frac{4R_s}{R_L}
\]  

(7)

And

\[
A v = \frac{2g_m R_L}{2a}
\]  

(8)

\[
R_{in} = 2R_s = \frac{2}{2g_m} = \frac{1}{g_m}
\]  

(9)

In this case, F is reduced and the effective transconductance is increased with a concomitant decrease in power dissipation.

III. BASIC IDEA

The use of capacitors does not increase PDC but A is set to 1 for minimum NF, \( g_m \) is restricted to 10 mS for input matching, reducing the gain in order to achieve high gain and low NF. A positive feedback can be inserted along with the negative feedback. But in the previous research pmos transistor is always used (Figure 3) [8], [9]. The idea in this paper is to use nmos type instead of pmos type (Figure 4), because of following reasons:

1 - pmos transistor should have larger size than nmos type to reach the same transconductance that leads to increase parasitic capacitor which causes to decrease bandwidth. Consequently, in proposed structure the larger bandwidth is obtained in previous works.

2 - as shown in Figure 4, since by placing nmos transistor at the input, indeed it uses current reuse technique which leads to reduce power consumption.

This feedback has the effect of increasing the input impedance:

\[
R_{in} = 2R_s = \frac{2}{2g_m (1 - R_L \beta g_m)}
\]  

(10)

This feedback affects the input impedance and does not influence the value of transconductance coefficient. Assuming
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\[ A_{pos} = R_L \beta \text{gm}_2 \], which varies from 0 to 1 for stability and \( A_{pos} \) can be 0 to 1 for an arbitrary choice of \( \text{gm}_1 \) to achieve an input matching condition. So the impedance matching does not set transistor biasing current and the current is variable to reduce noise. For example, suppose that:

\[ A_{NEG} = 1, \quad A_{pos} = 0.5, \quad R_s = 50 \quad (11) \]

According to above, \( \text{gm}_1 = 20 \text{mS} \), thus, the gain increases. Considering the thermal channel noise under input matching condition, the \( F \) is given by:

\[ F = 1 + \frac{1 - A_{pos} \gamma}{1 + A_{NEG} a} + \text{gm}_2 R_2 \frac{\gamma}{a} + \frac{R_a}{R_L} (2 - A_{pos})^2 \quad (12) \]

According to Equation 10 and 11, we have:

\[ A_v = 2 \text{gm}_1 R_L \quad (13) \]

\[ R_{in} = 2R_s = \frac{2}{\text{gm}_2} \quad (14) \]

\[ F = 1 + \frac{\gamma}{4a} + \text{gm}_2 R_s \frac{\gamma}{a} + \frac{9R_s}{4R_L} \quad (15) \]

The third term in Equation 15 represents the noise due to \( M_2 \) and can be decreased by using small \( \text{gm}_2 \) thus the combination of negative and the positive feedback have more power consumption that can decrease noise when compared to negative feedback alone with higher gain.

IV. PROPOSED LNA

Now, instead of bulky inductor that uses more area, we use current sources (M3) that are capacitive coupled \( C_3 \gg C_{gs3} \) (Figure 5) [10], [11].

The capacitively coupled M3 creates another positive current feedback. Besides small occupation area another freedom degree of input matching condition is provided.

So, there will be more flexibility in choosing the best value of the LNA transconductance which achieve minimum NF.

A. Input impedance

\[ R_{in} = 2R_s = \frac{2}{2 \text{gm}_1 (1 - R_L \beta \text{gm}_2) C_{gm3}} \quad (16) \]

Assuming \( A_{pos} = R_L \beta \text{gm}_2, \beta_{pos} = \frac{C_{gm2}}{2 \text{gm}_2} \), and \( A_{NEG} = 1 \), so we have:

\[ R_{in} = 2R_s = \frac{2}{2 \text{gm}_1 (1 - A_{pos} - \beta_{pos})} \quad (17) \]

Thus, the input matching condition is given by:

\[ 2 \text{gm}_1 R_s (1 - A_{pos} - \beta_{pos}) = 1 \quad (18) \]

From Equation 18, two degrees of freedom, \( A_{pos} \) and \( \beta_{pos} \), exist that allow arbitrary choice of \( \text{gm}_1 \) achieving high gain and low NF.

B. Noise analysis

For noise analyses, we draw noise current sources that due to the thermal noise of the transistors, load, and source resistance as shown in Fig.6 and replace the capacitors by short circuit since they are much larger than the capacitance of input transistors M1 and M3.

\[ \text{The output differential current due to each noise source is given by:} \]
Thermal noise due to the source resistance:

\[ i_{\text{ns-out}}^2 = A_k T R_s g m_i^2 \Delta f \]  

(19)

Thermal noise due to the M1:

\[ i_{\text{n1-out}}^2 = 4kT \gamma_2 \gamma_1 g m_i (g m_i R_S - 1)^2 \Delta f \]  

(20)

Thermal noise due to the M2:

\[ i_{\text{n2-out}}^2 = 4kT \gamma_2 \gamma_1 g m_2 (g m_2 R_S)^2 \Delta f \]  

(21)

Thermal noise due to the M3:

\[ i_{\text{n3-out}}^2 = 4kT \gamma_3 \gamma_1 g m_3 (g m_3 R_S)^2 \Delta f \]  

(22)

Assuming \( \gamma_1 = \gamma_2 = \gamma_3 = \gamma \), the noise factor is given by:

\[
F = \frac{i_{\text{total-out}}^2}{i_{\text{n-out}}^2} = 1 + \frac{\gamma (g m_i R_s - 1)^2}{a g m_i R_s} + \frac{\gamma g m_2 R_s}{a} \frac{\gamma}{g m_2 R_s} + g m_2 R_s + \frac{R_s}{R_L} \left( 1 + \frac{1}{2 g m_i R_s} \right)^2 
\]  

(23)

Under the input matching condition:

\[
2 g m_i R_s (1 - A_{\text{pos}} - \beta_{\text{pos}}) = 1 \rightarrow 2 g m_i R_s (1 - A_{\text{pos}} - \frac{g m_3}{2 g m_i}) = 1 \rightarrow g m_3 R_s = 2 g m_i R_s - 1 - 2 g m_i R_s A_{\text{pos}} 
\]  

(24)

And assuming \( \eta = g m_i R_s \), the F is reduced to:

\[
F = 1 + \frac{\gamma (\eta - 1)^2}{a} + \frac{2 \gamma}{a} (1 - A_{\text{pos}}) \eta \\
- \frac{\gamma}{a} (1 - \frac{R_s}{R_L} A_{\text{pos}}) + \frac{R_s}{R_L} (1 + \frac{1}{2 \eta})^2 
\]  

(25)

To determine optimum value for designing, we will estimate the amount of \( \eta \)

\[
\frac{dF}{d\eta} = 0 \\
\eta_{\text{opt}} = \frac{1}{\sqrt{3 - 2 A_{\text{pos}}}} 
\]  

(26)

The third term in Equation 25 plays an important role in noise reduction and we can say that the combination of three feedbacks contributes to noise cancellation.

V. RESULTS

The LNA has been implemented in TSMC 0.18-um CMOS technology. The total schematic of the LNA with the output buffer, pad capacitor, and bonding wire inductor is shown in Figure 7. A buffer is used at the LNA output to drive the 50-Ω load of the measuring equipment. The core LNA consumes 1.65mA from 1.8 V supply. The layout of the design has been done in cadence in order to obtain the practical results. The layout is shown in Figure 8. Figure 9-15 show the post layout simulated S-parameters, voltage gain, NF, and IIP3, respectively. The S11 is lower than -10dB until 2GHZ (Figure 9). Figure 10 and 11 also show the measured output return loss and reverse isolation: S22 is below -10dB up to 2GHZ, while S12 is below -23dB across the band. The voltage gain is 20.35dB with a 3-dB bandwidth of 2.83 GHZ (Figure 13).The minimum NF is 2.62 dB at 913 MHZ (Figure 14). Two-tone testing is performed with 100MHZ spacing for third-order inter-modulation distortion which is shown in Fig.15.the measured IIP3 is -1.67 dBm.

Table 1 show the performance summary of this work and compares with previous published wideband LNAs. The FOM defined in [12] is adopted.

\[
FOM = \frac{BW(GHZ).GV(Lin).PIIP3(mW)}{P_{DC}(mW).(F_{Lin})} 
\]  

(27)

where:

\[
Av(dB) = 20\log GV_{Lin} 
\]  

(28)

\[
IIP3(dB) = 10\log \frac{P_{IIP3}}{1(mW)} 
\]  

(29)

\[
NF = 10\log F_{Lin} 
\]  

(30)

As shown in this table, the FOM of this work is better than other works, because it has low noise, low power consumption, high linearity, and high bandwidth simultaneously.
VI. CONCLUSION

In this paper, a wideband inductorless LNA for multiband multistandard receiver is proposed. It uses three feedback paths for choice gm value arbitrarily for input matching and end to tradeoff between noise and input power matching. Post-layout simulation results show a voltage gain of 20.5dB with a 3-dB bandwidth of 3.19GHZ. A minimum NF of 2.3dB and an IIP3 of -2.17dBm while dissipating 1.65mA from 1.8V supply.
Table I
Comparison with recently published LNA

<table>
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<tr>
<th>Ref.</th>
<th>Gain (dB)</th>
<th>BW (GHz)</th>
<th>NF (dB)</th>
<th>IIP3 (dBm)</th>
<th>P_{dc} (mW)</th>
<th>Tech</th>
<th>FOM</th>
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<tr>
<td>[13]</td>
<td>16.9</td>
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<td>3.5</td>
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<td>um</td>
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<tr>
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<td>nm</td>
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This work (p nasty)

|         | 20.4      | -2.84    | 0.005   | 2.62       | -1.67     | 2.97  | 0.18 | 8.33 |

REFERENCES


